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PATENT ABSTRACTS OF JAPAN

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(54) DIGITAL SIGNAL PROCESSOR

(57)Abstract:
PROBLEM TO BE SOLVED: To raise a resolution with the relatively small increase of a circuit scale and power consumption.
SOLUTION: This digital signal processor for converting discrete signals sampled by a prescribed frequency ck to digital signals is provided with a dither signal generation means 6 for generating the dither signals of the same cycle as the discrete signals, an analog/digital conversion means 8 and a digital integration means 9. After adding the dither signals to the discrete signals, they are converted to the digital signals in the analog/digital conversion means 8 by using the clock signals of the frequency nck of (n)-folds (n is an integer ≥ 2) of the frequency of the discrete signals and the digital signals obtained on the output side of the analog/digital conversion means 8 are integrated for (n) times by the digital integration means 9 and outputted.

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CLAIMS

[Claim(s)]

[Claim 1] In the digital signal processor which changes into a digital signal the discrete signal sampled with predetermined frequency ck A dither signal generating means to generate the dither signal of the same period as said discrete signal, An analog-to-digital means and a digital integral means are established. While changing into a digital signal with said analog-to-digital means using a clock signal twice [n (n is two or more integers)] the frequency nck of the frequency of said discrete signal after adding said dither signal to said discrete signal The digital signal processor characterized by making it output after integrating with the digital signal acquired by the output side of said analog-to-digital means n times with said digital integral means.

[Claim 2] The digital signal processor characterized by said dither signal being a saw-tooth wave signal in a digital signal processor according to claim 1.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention is used for changing into a digital signal the discrete signal acquired by output sides, such as a CCD line sensor, and relates to a suitable digital signal processor.

[0002]

[Description of the Prior Art] For example, the flash plate (juxtaposition) mold analog-digital converter which is an analog-digital converter for high speeds is used for changing into a digital signal the discrete signal generally acquired by output sides, such as a CCD line sensor.

[0003] Conventionally, the thing with a resolving power of 10 bits is used as this flash plate (juxtaposition) mold analog-digital converter. 1024 comparators are required, a flash plate (juxtaposition) mold analog-digital converter with a resolving power [this] of

10 bits has a comparatively large circuit scale (chip area), and its power consumption is also comparatively large.
[0004] Since the circuit scale (chip area) became these twice and power consumption also became these twice when 1 more bit of resolving power of a flash plate (juxtaposition) mold analog-digital converter with a resolving power [this] of 10 bits was raised, there was un-arranging with difficult implementation of high-resolution-izing.
[0005] This invention aims at attaining high-resolution-ization by the increment in comparatively few circuit scales and power consumption in view of ******.
[0006]
[Means for Solving the Problem] In the digital signal processor from which this invention digital signal processor changes into a digital signal the discrete signal sampled with predetermined frequency ck A dither signal generating means to generate the dither signal of the same period as this discrete signal, After establishing an analog-to-digital means and a digital integral means and adding this dither signal to this discrete signal While changing into a digital signal with an analog-to-digital means using a clock signal twice [n (n is two or more integers)] the frequency nck of the frequency of this discrete signal It is made to output after integrating with the digital signal acquired by the output side of this analog-to-digital means n times with this digital integral means.
[0007] After adding the dither signal of for example, a saw-tooth wave signal to a discrete signal according to this invention, the clock signal of one n times, for example, 4 times, the frequency nck of the frequency of this discrete signal of this is used. Since it has changed into the digital signal with the analog-to-digital means, n pieces, for example, four pieces, for example, a 10-bit digital signal, are obtained one period of this discrete signal. Since he is trying to output this n digital signal, for example, four pieces, with a digital integral means times [n], for example, after finding the integral 4 times One n times, for example, 4 times, the resolution of this analog-to-digital means of this can be raised. For example, when the resolving power of this analog-to-digital means is 10 bits, a 12-bit digital signal can be outputted, and moreover, there are comparatively few increments in a circuit scale and power consumption.
[0008]
[Embodiment of the Invention] With reference to a drawing, I will explain per example of this invention digital signal processor below. In drawing 1 , 1 shows the optoelectric transducer which used CCD and this optoelectric transducer 1 is made as [acquire / the image pick-up signal which the signal which changes from field through period 1b and signal period 1c which are made into **** reset period 1a shown in drawing 2 A and reference level according to a clock signal ck to that output side repeats].
[0009] The image pick-up signal acquired by the output side of this optoelectric transducer 1 is supplied to the correlation duplex sampling circuit 2.
[0010] Moreover, 3 shows the clock generation circuit which generates clock signal 4ck 4 times the frequency of the clock signal ck supplied to an optoelectric transducer 1, and carries out it as [supply / through 1/4 counting-down circuit 4 / clock signal 4ck of this clock generation circuit 3 / to an optoelectric transducer 1 / as a clock signal ck].
[0011] Moreover, the correlation duplex sampling circuit 2 is supplied by making into a sampling signal the clock signal ck acquired by the output side of this 1/4 counting-down circuit 4. In this correlation duplex sampling circuit 2, it carries out as [obtain / discrete-signal 2a sampled on the frequency ck of an opposite phase as level of field through

period 1b was made into reference level, the sampling hold of the level of signal period 1c was carried out and it was shown in drawing 2 B]. It carries out as [supply / to an adder circuit 5 / discrete-signal 2a obtained by the output side of this correlation duplex sampling circuit 2].

[0012] Moreover, 6 shows a dither signal generating circuit, and as this example is shown in drawing 2 C as this dither signal, it is taken as saw-tooth wave signal 6a of the same period as discrete-signal 2a shown in drawing 2 B. Level of the peak two peak of this saw-tooth wave signal 6a is carried out as [consider / as three fourths of the level of 1 quantization level (LSB) of the analogue-to-digital conversion circuit 8 mentioned later].

 [0013] It carries out as [supply / to an adder circuit 5 / saw-tooth wave signal 6a of the same period as discrete-signal 2a obtained by the output side of this dither signal generating circuit 6]. In this adder circuit 5, saw-tooth wave signal 6a which is a dither signal is added to this discrete-signal 2a, and as shown in drawing 2 D, the signal with which saw-tooth wave signal 6a which is a dither signal was added to this discrete-signal 2a is acquired by the output side of this adder circuit 5.

[0014] The signal with which saw-tooth wave signal 6a which is a dither signal was added to discrete-signal 2a obtained by the output side of this adder circuit 5 is supplied to the sampling hold circuit 7. In this sampling hold circuit 7, by making into a sampling signal clock signal 4ck 4 times the frequency of the clock signal ck acquired in the clock generation circuit 3, a sampling hold is carried out and it carries out as [obtain / at the **** 1 clock-signal ck period shown in the output side of this sampling hold circuit 7 at drawing 2 E / the sampling hold signal which carried out the sampling hold 4 times].

[0015] The sampling hold signal obtained by the output side of this sampling hold circuit 7 is supplied to the analogue-to-digital conversion circuit 8. As this analogue-to-digital conversion circuit 8, a thing with a resolution of 10 bits is used in this example.

[0016] Moreover, in this example, this analogue-to-digital conversion circuit 8 is carried out as [change / by clock signal 4ck 4 times the frequency of the clock signal ck acquired in the clock generation circuit 3 / into a digital signal / an analog signal].

[0017] Therefore, the digital signal whose resolving power of four pieces is 10 bits is acquired by the output side of this analogue-to-digital conversion circuit 8 at a 1 clock-signal ck period. The resolving power obtained by the output side of this analogue-to-digital conversion circuit 8 supplies the digital signal which is 10 bits to digital adder 9a of 12 bit patterns which constitute the digital integrating circuit 9.

[0018] The output signal of this digital adder 9a is supplied to digital latch circuit 9b of 12 bit patterns which constitute this digital integrating circuit 9, and the output signal of this latch circuit 9b is supplied to digital adder 9a. While making it operate by clock signal 4ck 4 times the frequency of the clock signal ck acquired as a clock signal of this latch circuit 9b in the clock generation circuit 3, a clock signal ck is supplied to the clear terminal cl, and it carries out as [clear / this / this latch circuit 9b].

[0019] That is, this digital integrating circuit 9 is a thing the bottom which carries out the digital integral of the four digital signals of a 1 clock-signal ck period. It becomes the **** integral wave which shows the output signal of this digital adder 9a to drawing 2 F when a signal wave form is observed through the digital-to-analog circuit of 12 bit patterns.

[0020] The output signal of this digital adder 9a is supplied to the digital latch circuit 10 of 12 bit patterns. The clock signal of a frequency ck is supplied to this latch circuit 10 as

a clock signal. That is, sequential supply of the signal with which the digital output signal of the analogue-to-digital conversion circuit 8 integrated 4 times is carried out at this latch circuit 10.
[0021] It carries out as [supply / to the digital video-signal output terminal 11 of 12 bit patterns / the output signal of this latch circuit 10]. The signal corresponding to the signal which was in discrete-signal 2a which shows the output signal of this latch circuit 10 to drawing 2 B as shown in drawing 2 G when a signal wave form is observed through the digital-to-analog circuit of 12 bit patterns during the 1 clock-signal ck was acquired.
[0022] Furthermore, with reference to drawing 3 and drawing 4 , it explains to a detail in simulation about actuation of this analogue-to-digital conversion circuit 8 of this example, the digital integrating circuit 9, and a latch circuit 10.
[0023] As shown in drawing 3 , whenever the level of the analog signal inputted generally exceeds 1 quantization level (LSB) in 1 sampling period (1 clock-signal ck period) in an analogue-to-digital conversion circuit, digital value carries out "1" step rise. The analogue-to-digital conversion circuit 8 with a resolving power [this] of 10 bits is the resolving power of 1024 steps.
[0024] By the way, it sets to this example. A peak two peak level the analog signal supplied to the input side of this analogue-to-digital conversion circuit 8 to discrete-signal 2a obtained by the output side of the correlation duplex sampling circuit 2 as three fourths of dither signals of level of 1 quantization level (LSB) In four **** which are the signals with which ********** signal 6a was added, and are shown in drawing 4 A for each step of every of these 1024 steps, it is a1 -a4. It thinks.
[0025] namely, a case -- a1 like -- the time of being the level of 0 - 1/4 of 1 quantization level (LSB) of a step with discrete-signal 2a -- 4 times as much clock signal 4ck as a clock signal ck -- one by one -- 4 times C1, C2, and C3 C4 [and] -- the case where 1 quantization level is not exceeded once even if it carries out a sampling hold in the sampling hold circuit 7 -- a case -- a2 like -- a discrete signal in the time of the level of 1 / 4 - 2/4 of 1 quantization level (LSB) of a certain step the case where it exceeds once -- a case -- a3 like -- a discrete signal in the time of the level of 2 / 4 - 3/4 of 1 quantization level (LSB) of a certain step a case when exceeding twice -- a4 like -- a discrete signal is the case where it exceeds 3 times in the time of less than 3 / four to 1 level of 1 quantization level (LSB) of a certain step (refer to drawing 4 B).
[0026] In the case of four, the digital signal which looks at that component value in analog, and is acquired by drawing 4 C at ** [like] and this latch circuit 10 when the digital integrating circuit 9 is integrated with the output of this analogue-to-digital conversion circuit 8 4 times is a1 -a4 at each step of 1024 steps. The digital signal of 4096 steps which have resolving power is acquired, and resolving power serves as the analogue-to-digital conversion circuit and equivalence which are 12 bits.
[0027] After adding the dither signal of saw-tooth wave signal 6a to discrete-signal 2a which sampled the image pick-up signal on the frequency ck according to this example Since it has changed into the digital signal by the analogue-to-digital conversion circuit 8 using the 4 times as many clock signal of frequency 4ck as the frequency of this discrete-signal 2a Since he is trying to output after acquiring four 10-bit digital signals one period of this discrete-signal 2a and integrating the digital integrating circuit 9 with this four digital signal 4 times A digital signal with a conversion circuit [this / 8 / 4 times the resolving power of an analogue to digital] and a resolving power of 12 bits is acquired.

[0028] Since the digital integrating circuit 9 and a latch circuit 10 only increase as a circuit scale as compared with the conventional analogue-to-digital conversion circuit according to this example, as for the increment in this circuit scale, the increment in power consumption also has comparatively few profits comparatively few therefore. For this reason, according to this example, the analog-to-digital means of a high resolution can be realized comparatively cheaply.
[0029] Moreover, according to this example, the dither signal is added at the time of an analog to digital, but since the digital integrating circuit 9 is integrated, there are profits which fluctuation of an output signal does not produce.
[0030] In addition, although it stated so that the dither signal generating circuit 6 where a peak two peak generates serration wave signal 6a of 3/4LSB might be formed in drawing 1 , as it is shown in drawing 5 , it is the capacitor C3 for a hold of the correlation duplex sampling circuit 2. It is Resistor RX to juxtaposition. It prepares and is this capacitor C3. Resistor RX The time constant to depend may be carried out as [serve as / a ripple / abbreviation 3 / 4LSB].
[0031] Per this drawing 5 and also the **** image pick-up signal which 20 shows the input terminal of the correlation duplex sampling hold circuit 2 for stating, and is shown [state] in this input terminal 20 in this drawing 5 at drawing 2 A are supplied. It connects with the 1 side of sampling switch 22a which turns on this input terminal 20 by the sampling pulse ck in signal period 1c of an image pick-up signal through the connection switch 21 switch on only in field through period 1b which is the reference signal of this image pick-up signal.
[0032] It is the capacitor C1 for a reference voltage hold about the node of this connection switch 21 and sampling switch 22a. It minds and grounds. while connecting a side besides this sampling switch 22a to non-inversed input terminal + of the operation amplifying circuit 23 which constitutes a comparator circuit -- this non-inversed input terminal + -- capacitor C3 for a reference voltage hold while minding and grounding -- this capacitor C3 the ripple according to a time constant to juxtaposition -- about -- resistor RX used as 3/4LSB It carries out as [connect].
[0033] Moreover, while connecting with inversed input terminal - of the operation amplifying circuit 23 through sampling switch 22b which turns on this input terminal 20 by the sampling pulse ck in signal period 1c of an image pick-up signal, it is this inversed input terminal. - Capacitor C2 for a sampling hold It minds and connects. An output terminal 24 is derived from this operation amplifying circuit 23.
[0034] In this drawing 5 , when the **** image pick-up signal shown in an input terminal 20 at drawing 2 A is supplied, **** shown in drawing 2 D and the signal with which the dither signal of a saw-tooth wave signal was added to the discrete signal with which the sampling hold of the signal period 1c of an image pick-up signal was carried out are acquired by the output terminal 24.
[0035] Moreover, although the sampling hold circuit 7 was formed in the example of drawing 1 , the analogue-to-digital conversion circuit 8 can be a flash plate mold, or can omit this sampling hold circuit 7 in what builds in the sampling hold circuit in this analogue-to-digital conversion circuit 8.
[0036] Moreover, although it stated so that an analog to digital might be carried out in the above-mentioned example with a clock signal 4 times the frequency of the frequency ck of a discrete signal, the frequency of this clock signal can use a n times (n is two or more

integers) as many thing as this, and can make it one n times the resolution of this at this time.
[0037] Moreover, as for this invention, it is needless to say that various configurations can take in addition to this, without deviating from the summary of this invention, without restricting to the above-mentioned example.
[0038]
[Effect of the Invention] According to this invention, as compared with the conventional analogue-to-digital conversion circuit, there are profits which can obtain the analogue-to-digital inverter of a high resolution by the increment in a circuit scale only with only increasing [comparatively little] the digital integrating circuit 9 and a latch circuit 10 as a circuit scale.
[0039] Moreover, since there are few increments in a circuit scale according to this invention, there are profits from which the increment in power consumption can obtain the analogue-to-digital inverter of a high resolution that it is few and cheaply. Moreover, according to this invention, the dither signal is added at the time of an analog to digital, but since the digital integrator is integrated, there are profits which fluctuation of an output signal does not produce

TECHNICAL FIELD

[Field of the Invention] This invention is used for changing into a digital signal the discrete signal acquired by output sides, such as a CCD line sensor, and relates to a suitable digital signal processor.

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, as compared with the conventional analogue-to-digital conversion circuit, there are profits which can obtain the analogue-to-digital inverter of a high resolution by the increment in a circuit scale only with only increasing [comparatively little] the digital integrating circuit 9 and a latch circuit 10 as a circuit scale.
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TECHNICAL PROBLEM

[Description of the Prior Art] For example, the flash plate (juxtaposition) mold analog-digital converter which is an analog-digital converter for high speeds is used for changing into a digital signal the discrete signal generally acquired by output sides, such as a CCD

line sensor.
[0003] Conventionally, the thing with a resolving power of 10 bits is used as this flash plate (juxtaposition) mold analog-digital converter. 1024 comparators are required, a flash plate (juxtaposition) mold analog-digital converter with a resolving power [this] of 10 bits has a comparatively large circuit scale (chip area), and its power consumption is also comparatively large.
[0004] Since the circuit scale (chip area) became these twice and power consumption also became these twice when 1 more bit of resolving power of a flash plate (juxtaposition) mold analog-digital converter with a resolving power [this] of 10 bits was raised, there was un-arranging with difficult implementation of high-resolution-izing.
[0005] This invention aims at attaining high-resolution-ization by the increment in comparatively few circuit scales and power consumption in view of ******.

MEANS

[Means for Solving the Problem] In the digital signal processor from which this invention digital signal processor changes into a digital signal the discrete signal sampled with predetermined frequency ck A dither signal generating means to generate the dither signal of the same period as this discrete signal, After establishing an analog-to-digital means and a digital integral means and adding this dither signal to this discrete signal While changing into a digital signal with an analog-to-digital means using a clock signal twice [n (n is two or more integers)] the frequency nck of the frequency of this discrete signal It is made to output after integrating with the digital signal acquired by the output side of this analog-to-digital means n times with this digital integral means.
[0007] After adding the dither signal of for example, a saw-tooth wave signal to a discrete signal according to this invention, the clock signal of one n times, for example, 4 times, the frequency nck of the frequency of this discrete signal of this is used. Since it has changed into the digital signal with the analog-to-digital means, n pieces, for example, four pieces, for example, a 10-bit digital signal, are obtained one period of this discrete signal. Since he is trying to output this n digital signal, for example, four pieces, with a digital integral means times [n], for example, after finding the integral 4 times One n times, for example, 4 times, the resolution of this analog-to-digital means of this can be raised. For example, when the resolving power of this analog-to-digital means is 10 bits, a 12-bit digital signal can be outputted, and moreover, there are comparatively few increments in a circuit scale and power consumption.
[0008]
[Embodiment of the Invention] With reference to a drawing, I will explain per example of this invention digital signal processor below. In drawing 1 , 1 shows the optoelectric transducer which used CCD and this optoelectric transducer 1 is made as [acquire / the image pick-up signal which the signal which changes from field through period 1b and signal period 1c which are made into **** reset period 1a shown in drawing 2 A and reference level according to a clock signal ck to that output side repeats].
[0009] The image pick-up signal acquired by the output side of this optoelectric transducer 1 is supplied to the correlation duplex sampling circuit 2.
[0010] Moreover, 3 shows the clock generation circuit which generates clock signal 4ck 4

times the frequency of the clock signal ck supplied to an optoelectric transducer 1, and carries out it as [supply / through 1/4 counting-down circuit 4 / clock signal 4ck of this clock generation circuit 3 / to an optoelectric transducer 1 / as a clock signal ck].

[0011] Moreover, the correlation duplex sampling circuit 2 is supplied by making into a sampling signal the clock signal ck acquired by the output side of this 1/4 counting-down circuit 4. In this correlation duplex sampling circuit 2, it carries out as [obtain / discrete-signal 2a sampled on the frequency ck of an opposite phase as level of field through period 1b was made into reference level, the sampling hold of the level of signal period 1c was carried out and it was shown in drawing 2 B]. It carries out as [supply / to an adder circuit 5 / discrete-signal 2a obtained by the output side of this correlation duplex sampling circuit 2].

[0012] Moreover, 6 shows a dither signal generating circuit, and as this example is shown in drawing 2 C as this dither signal, it is taken as saw-tooth wave signal 6a of the same period as discrete-signal 2a shown in drawing 2 B. Level of the peak two peak of this saw-tooth wave signal 6a is carried out as [consider / as three fourths of the level of 1 quantization level (LSB) of the analogue-to-digital conversion circuit 8 mentioned later].

[0013] It carries out as [supply / to an adder circuit 5 / saw-tooth wave signal 6a of the same period as discrete-signal 2a obtained by the output side of this dither signal generating circuit 6]. In this adder circuit 5, saw-tooth wave signal 6a which is a dither signal is added to this discrete-signal 2a, and as shown in drawing 2 D, the signal with which saw-tooth wave signal 6a which is a dither signal was added to this discrete-signal 2a is acquired by the output side of this adder circuit 5.

[0014] The signal with which saw-tooth wave signal 6a which is a dither signal was added to discrete-signal 2a obtained by the output side of this adder circuit 5 is supplied to the sampling hold circuit 7. In this sampling hold circuit 7, by making into a sampling signal clock signal 4ck 4 times the frequency of the clock signal ck acquired in the clock generation circuit 3, a sampling hold is carried out and it carries out as [obtain / at the **** 1 clock-signal ck period shown in the output side of this sampling hold circuit 7 at drawing 2 E / the sampling hold signal which carried out the sampling hold 4 times].

[0015] The sampling hold signal obtained by the output side of this sampling hold circuit 7 is supplied to the analogue-to-digital conversion circuit 8. As this analogue-to-digital conversion circuit 8, a thing with a resolution of 10 bits is used in this example.

[0016] Moreover, in this example, this analogue-to-digital conversion circuit 8 is carried out as [change / by clock signal 4ck 4 times the frequency of the clock signal ck acquired in the clock generation circuit 3 / into a digital signal / an analog signal].

[0017] Therefore, the digital signal whose resolving power of four pieces is 10 bits is acquired by the output side of this analogue-to-digital conversion circuit 8 at a 1 clock-signal ck period. The resolving power obtained by the output side of this analogue-to-digital conversion circuit 8 supplies the digital signal which is 10 bits to digital adder 9a of 12 bit patterns which constitute the digital integrating circuit 9.

[0018] The output signal of this digital adder 9a is supplied to digital latch circuit 9b of 12 bit patterns which constitute this digital integrating circuit 9, and the output signal of this latch circuit 9b is supplied to digital adder 9a. While making it operate by clock signal 4ck 4 times the frequency of the clock signal ck acquired as a clock signal of this latch circuit 9b in the clock generation circuit 3, a clock signal ck is supplied to the clear terminal cl, and it carries out as [clear / this / this latch circuit 9b].

[0019] That is, this digital integrating circuit 9 is a thing the bottom which carries out the digital integral of the four digital signals of a 1 clock-signal ck period. It becomes the **** integral wave which shows the output signal of this digital adder 9a to drawing 2 F when a signal wave form is observed through the digital-to-analog circuit of 12 bit patterns.
[0020] The output signal of this digital adder 9a is supplied to the digital latch circuit 10 of 12 bit patterns. The clock signal of a frequency ck is supplied to this latch circuit 10 as a clock signal. That is, sequential supply of the signal with which the digital output signal of the analogue-to-digital conversion circuit 8 integrated 4 times is carried out at this latch circuit 10.
[0021] It carries out as [supply / to the digital video-signal output terminal 11 of 12 bit patterns / the output signal of this latch circuit 10]. The signal corresponding to the signal which was in discrete-signal 2a which shows the output signal of this latch circuit 10 to drawing 2 B as shown in drawing 2 G when a signal wave form is observed through the digital-to-analog circuit of 12 bit patterns during the 1 clock-signal ck was acquired.
[0022] Furthermore, with reference to drawing 3 and drawing 4 , it explains to a detail in simulation about actuation of this analogue-to-digital conversion circuit 8 of this example, the digital integrating circuit 9, and a latch circuit 10.
[0023] As shown in drawing 3 , whenever the level of the analog signal inputted generally exceeds 1 quantization level (LSB) in 1 sampling period (1 clock-signal ck period) in an analogue-to-digital conversion circuit, digital value carries out "1" step rise. The analogue-to-digital conversion circuit 8 with a resolving power [this] of 10 bits is the resolving power of 1024 steps.
[0024] By the way, it sets to this example. A peak two peak level the analog signal supplied to the input side of this analogue-to-digital conversion circuit 8 to discrete-signal 2a obtained by the output side of the correlation duplex sampling circuit 2 as three fourths of dither signals of level of 1 quantization level (LSB) In four **** which are the signals with which ********** signal 6a was added, and are shown in drawing 4 A for each step of every of these 1024 steps, it is a1 -a4. It thinks.
[0025] namely, a case -- a1 like -- the time of being the level of 0 - 1/4 of 1 quantization level (LSB) of a step with discrete-signal 2a -- 4 times as much clock signal 4ck as a clock signal ck -- one by one -- 4 times C1, C2, and C3 C4 [and] -- the case where 1 quantization level is not exceeded once even if it carries out a sampling hold in the sampling hold circuit 7 -- a case -- a2 like -- a discrete signal in the time of the level of 1 / 4 - 2/4 of 1 quantization level (LSB) of a certain step the case where it exceeds once -- a case -- a3 like -- a discrete signal in the time of the level of 2 / 4 - 3/4 of 1 quantization level (LSB) of a certain step a case when exceeding twice -- a4 like -- a discrete signal is the case where it exceeds 3 times in the time of less than 3 / four to 1 level of 1 quantization level (LSB) of a certain step (refer to drawing 4 B).
[0026] In the case of four, the digital signal which looks at that component value in analog, and is acquired by drawing 4 C at ** [like] and this latch circuit 10 when the digital integrating circuit 9 is integrated with the output of this analogue-to-digital conversion circuit 8 4 times is a1 -a4 at each step of 1024 steps. The digital signal of 4096 steps which have resolving power is acquired, and resolving power serves as the analogue-to-digital conversion circuit and equivalence which are 12 bits.
[0027] After adding the dither signal of saw-tooth wave signal 6a to discrete-signal 2a

which sampled the image pick-up signal on the frequency ck according to this example Since it has changed into the digital signal by the analogue-to-digital conversion circuit 8 using the 4 times as many clock signal of frequency 4ck as the frequency of this discrete-signal 2a Since he is trying to output after acquiring four 10-bit digital signals one period of this discrete-signal 2a and integrating the digital integrating circuit 9 with this four digital signal 4 times A digital signal with a conversion circuit [this / 8 / 4 times the resolving power of an analogue to digital] and a resolving power of 12 bits is acquired.
[0028] Since the digital integrating circuit 9 and a latch circuit 10 only increase as a circuit scale as compared with the conventional analogue-to-digital conversion circuit according to this example, as for the increment in this circuit scale, the increment in power consumption also has comparatively few profits comparatively few therefore. For this reason, according to this example, the analog-to-digital means of a high resolution can be realized comparatively cheaply.
[0029] Moreover, according to this example, the dither signal is added at the time of an analog to digital, but since the digital integrating circuit 9 is integrated, there are profits which fluctuation of an output signal does not produce.
[0030] In addition, although it stated so that the dither signal generating circuit 6 where a peak two peak generates serration wave signal 6a of 3/4LSB might be formed in drawing 1 , as it is shown in drawing 5 , it is the capacitor C3 for a hold of the correlation duplex sampling circuit 2. It is Resistor RX to juxtaposition. It prepares and is this capacitor C3. Resistor RX The time constant to depend may be carried out as [serve as / a ripple / abbreviation 3 / 4LSB].
[0031] Per this drawing 5 and also the **** image pick-up signal which 20 shows the input terminal of the correlation duplex sampling hold circuit 2 for stating, and is shown [state] in this input terminal 20 in this drawing 5 at drawing 2 A are supplied. It connects with the 1 side of sampling switch 22a which turns on this input terminal 20 by the sampling pulse ck in signal period 1c of an image pick-up signal through the connection switch 21 switch on only in field through period 1b which is the reference signal of this image pick-up signal.
[0032] It is the capacitor C1 for a reference voltage hold about the node of this connection switch 21 and sampling switch 22a. It minds and grounds. while connecting a side besides this sampling switch 22a to non-inversed input terminal + of the operation amplifying circuit 23 which constitutes a comparator circuit -- this non-inversed input terminal + -- capacitor C3 for a reference voltage hold while minding and grounding -- this capacitor C3 the ripple according to a time constant to juxtaposition -- about -- resistor RX used as 3/4LSB It carries out as [connect].
[0033] Moreover, while connecting with inversed input terminal - of the operation amplifying circuit 23 through sampling switch 22b which turns on this input terminal 20 by the sampling pulse ck in signal period 1c of an image pick-up signal, it is this inversed input terminal. - Capacitor C2 for a sampling hold It minds and connects. An output terminal 24 is derived from this operation amplifying circuit 23.
[0034] In this drawing 5 , when the **** image pick-up signal shown in an input terminal 20 at drawing 2 A is supplied, **** shown in drawing 2 D and the signal with which the dither signal of a saw-tooth wave signal was added to the discrete signal with which the sampling hold of the signal period 1c of an image pick-up signal was carried out are acquired by the output terminal 24.

[0035] Moreover, although the sampling hold circuit 7 was formed in the example of drawing 1 , the analogue-to-digital conversion circuit 8 can be a flash plate mold, or can omit this sampling hold circuit 7 in what builds in the sampling hold circuit in this analogue-to-digital conversion circuit 8.
[0036] Moreover, although it stated so that an analog to digital might be carried out in the above-mentioned example with a clock signal 4 times the frequency of the frequency ck of a discrete signal, the frequency of this clock signal can use a n times (n is two or more integers) as many thing as this, and can make it one n times the resolution of this at this time.
[0037] Moreover, as for this invention, it is needless to say that various configurations can take in addition to this, without deviating from the summary of this invention, without restricting to the above-mentioned example

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing one example of this invention digital signal processor.
[Drawing 2] It is the diagram with which explanation of this invention is presented.
[Drawing 3] It is the diagram with which explanation is presented.
[Drawing 4] It is the diagram with which explanation of this invention is presented.
[Drawing 5] It is the block diagram showing other examples of the important section of this invention.
[Description of Notations]
1 Optoelectric Transducer, 2 Correlation Duplex Sampling Circuit, 3 Clock Generation Circuit, 4 1/4 Counting-down Circuit, 5 Adder Circuit, 6 Dither Signal Generating Circuit, 8 Analogue-to-Digital Conversion Circuit, 9 Digital Integrating Circuit, 10 Latch Circuit, 11 Output Terminal

DRAWINGS

DRAWINGS

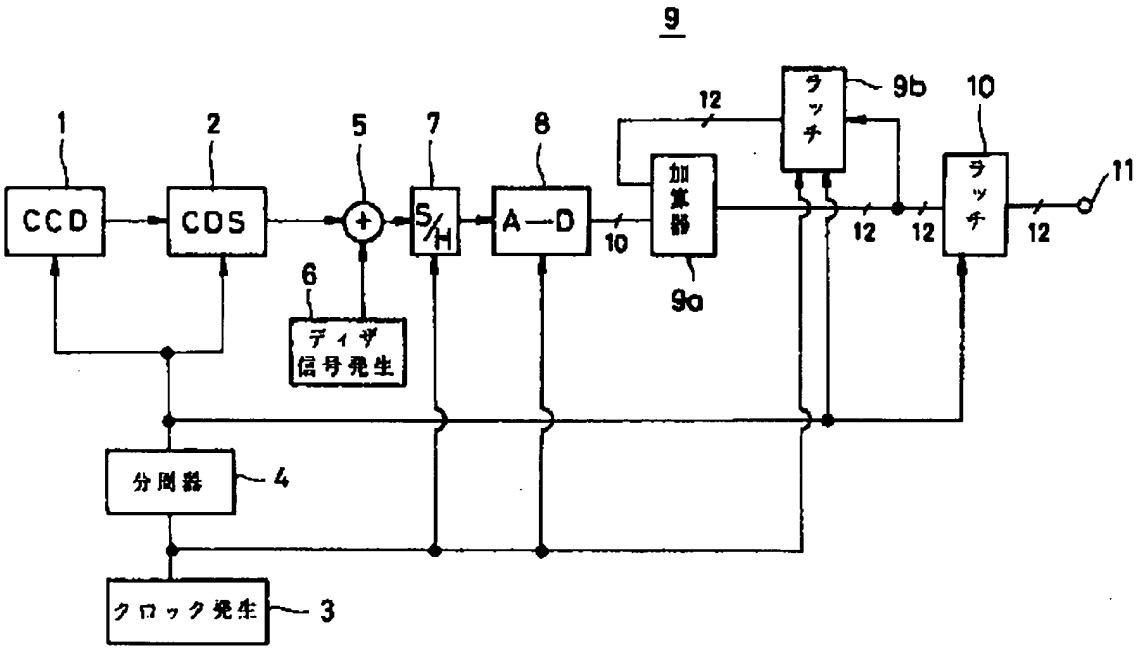

Figure 1

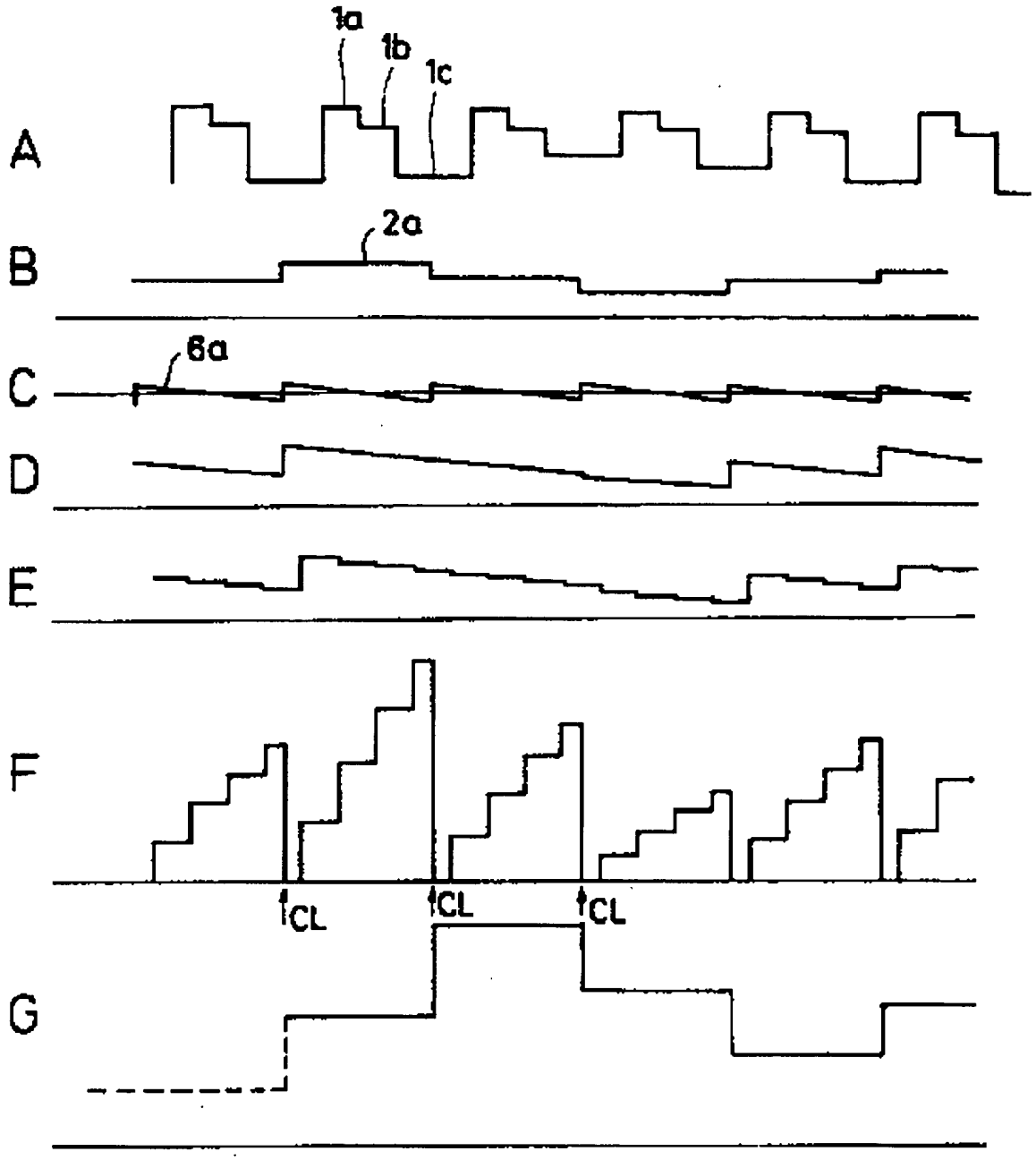

Figure 2

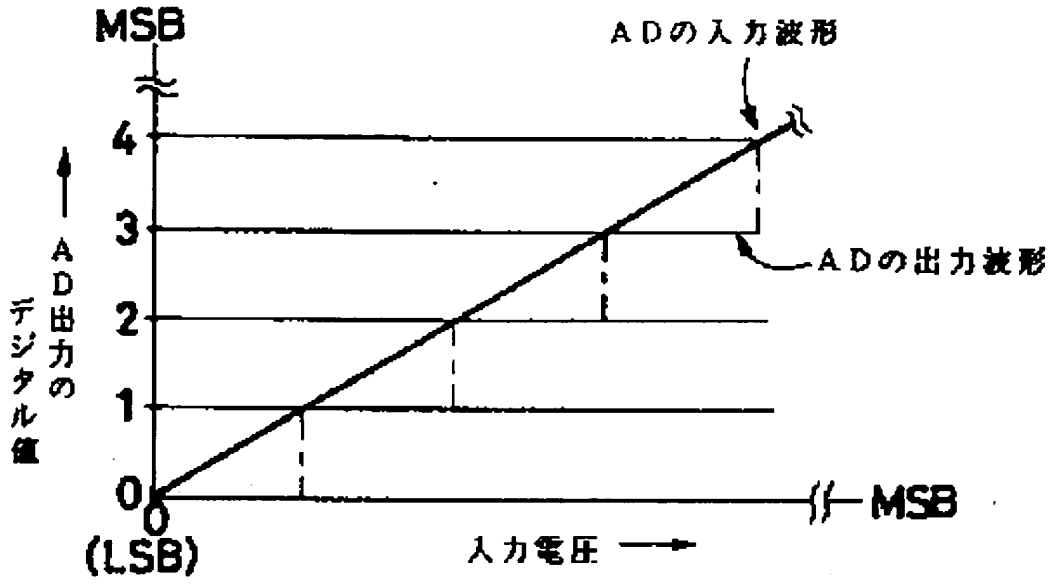

Figure 3

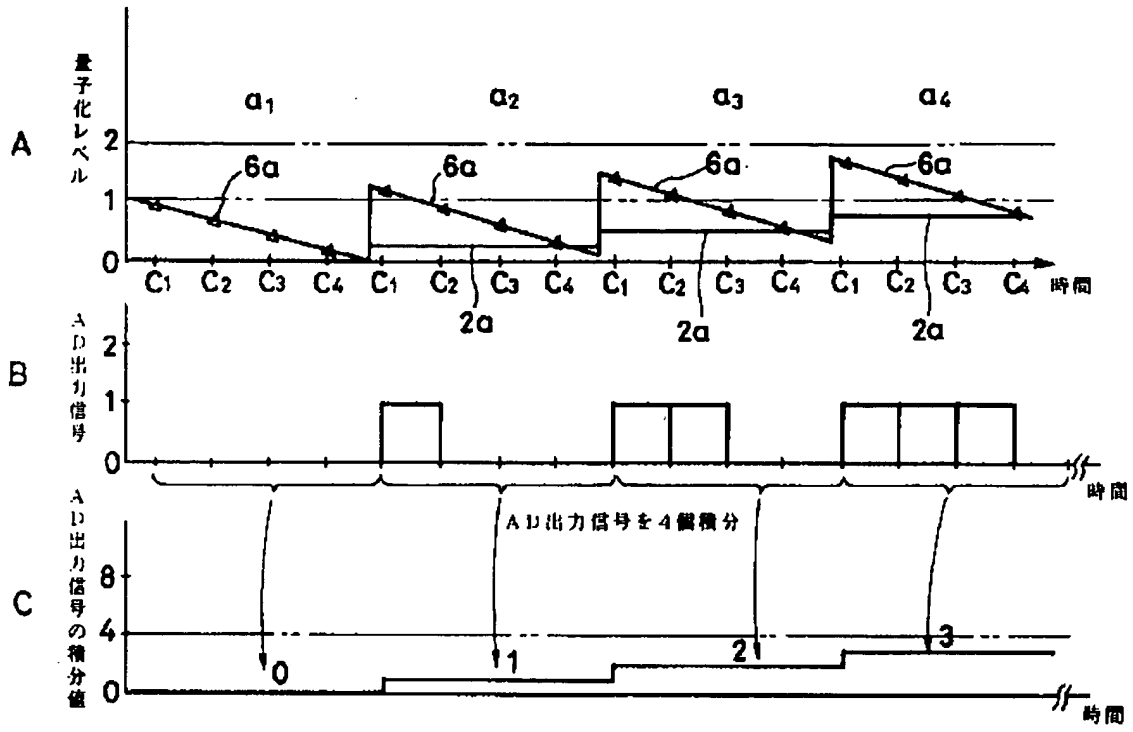
A
量子化レベル
2
1
0
a1
a2
a3
a4
6a
6a
6a
6a
C1 C2 C3 C4 C1 C2 C3 C4 C1 C2 C3 C4 C1 C2 C3 C4
時間
2a
2a
2a
B
AD出力信号
2
1
0
時間
AD出力信号を4個積分
C
AD出力信号の積分値
8
4
0
0
1
2
3
時間

Figure 4

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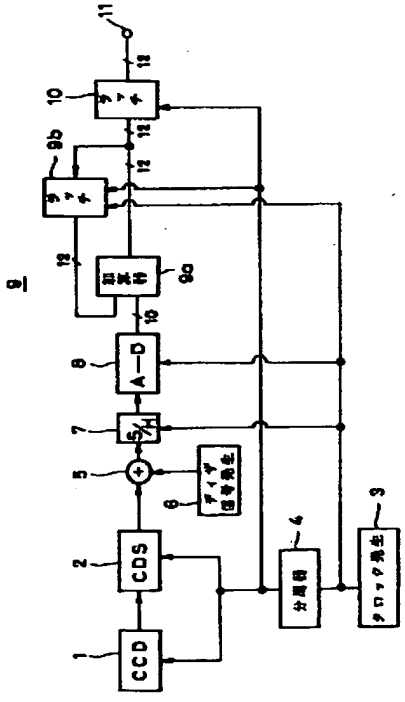
(54)【発明の名称】　デジタル信号処理装置

(57)【要約】

【課題】　比較的少ない回路規模及び消費電力の増加で高分解能化を図ることを目的とする。

【解決手段】　所定周波数ｃｋでサンプリングされた離散的信号をデジタル信号に変換するデジタル信号処理装置において、この離散的信号と同じ周期のディザ信号を発生するディザ信号発生手段と、アナログ－デジタル変換手段と、デジタル積分手段とを設け、この離散的信号にこのディザ信号を付加した後に、この離散的信号の周波数のｎ（ｎは２以上の整数）倍の周波数ｎｃｋのクロック信号を使用してアナログ－デジタル変換手段でデジタル信号に変換すると共にこのアナログ－デジタル変換手段の出力側に得られるデジタル信号をこのデジタル積分手段によりｎ回積分した後に出力するようにしたものである。



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【特許請求の範囲】

【請求項1】　所定周波数ｃｋでサンプリングされた離散的信号をデジタル信号に変換するデジタル信号処理装置において、

前記離散的信号と同じ周期のディザ信号を発生するディザ信号発生手段と、

アナログ－デジタル変換手段と、

デジタル積分手段とを設け、

前記離散的信号に前記ディザ信号を付加した後に前記離散的信号の周波数のｎ（ｎは2以上の整数）倍の周波数ｎｃｋのクロック信号を使用して前記アナログ－デジタル変換手段でデジタル信号に変換すると共に前記アナログ－デジタル変換手段の出力側に得られるデジタル信号を前記デジタル積分手段によりｎ回積分した後に出力するようにしたことを特徴とするデジタル信号処理装置。

【請求項2】　請求項1記載のデジタル信号処理装置において、

前記ディザ信号が鋸歯状波信号であることを特徴とするデジタル信号処理装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＣＣＤラインセンサ等の出力側に得られる離散的信号をデジタル信号に変換するのに使用して好適なデジタル信号処理装置に関する。

【０００２】

【従来の技術及び発明が解決しようとする課題】一般にＣＣＤラインセンサ等の出力側に得られる離散的信号をデジタル信号に変換するのに高速用アナログ－デジタル変換器である例えばフラッシュ（並列）型アナログ－デジタル変換器が使用されている。

【０００３】従来、このフラッシュ（並列）型アナログ－デジタル変換器として例えば分解能１０ビットのものが使用されている。この分解能１０ビットのフラッシュ（並列）型アナログ－デジタル変換器は１０２４個のコンパレータが必要であり、回路規模（チップ面積）が比較的大きく、消費電力も比較的大きい。

【０００４】この分解能１０ビットのフラッシュ（並列）型アナログ－デジタル変換器の分解能を更に1ビット上げたときには、回路規模（チップ面積）が、この2倍となり、また消費電力もこの2倍となるので、高分解能化の実現が困難である不都合があった。

【０００５】本発明は斯る点に鑑み比較的少ない回路規模及び消費電力の増加で高分解能化を図ることを目的とする。

【０００６】

【課題を解決するための手段】本発明デジタル信号処理装置は所定周波数ｃｋでサンプリングされた離散的信号をデジタル信号に変換するデジタル信号処理装置において、この離散的信号と同じ周期のディザ信号を発生する

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ディザ信号発生手段と、アナログ－デジタル変換手段と、デジタル積分手段とを設け、この離散的信号にこのディザ信号を付加した後に、この離散的信号の周波数のｎ（ｎは2以上の整数）倍の周波数ｎｃｋのクロック信号を使用してアナログ－デジタル変換手段でデジタル信号に変換すると共にこのアナログ－デジタル変換手段の出力側に得られるデジタル信号をこのデジタル積分手段によりｎ回積分した後に出力するようにしたものである。

【０００７】本発明によれば、離散的信号に例えば鋸歯状波信号のディザ信号を付加した後に、この離散的信号の周波数のｎ倍例えば４倍の周波数ｎｃｋのクロック信号を使用して、アナログ－デジタル変換手段でデジタル信号に変換しているので、この離散的信号の１周期でｎ個例えば４個の例えば１０ビットのデジタル信号が得られ、このｎ個例えば４個のデジタル信号をデジタル積分手段によりｎ回例えば４回積分した後に出力するようにしているので、このアナログ－デジタル変換手段のｎ倍例えば４倍の分解能を上げることができ、例えばこのアナログ－デジタル変換手段の分解能が１０ビットであったときに例えば１２ビットのデジタル信号を出力することができ、しかも回路規模及び消費電力の増加は比較的少ない。

【０００８】

【発明の実施の形態】以下図面を参照して本発明デジタル信号処理装置の一実施例につき説明しよう。図1において、1はＣＣＤを使用した光電変換素子を示し、この光電変換素子1は、その出力側にクロック信号ｃｋに従って、図２Ａに示す如きリセット期間１ａ，基準レベルとするフィールドスルー期間１ｂ及び信号期間１ｃより成る信号が繰り返す撮像信号が得られる如くなされている。

【０００９】この光電変換素子1の出力側に得られる撮像信号を相関二重サンプリング回路2に供給する。

【００１０】また、3は光電変換素子1に供給するクロック信号ｃｋの４倍の周波数のクロック信号４ｃｋを発生するクロック発生回路を示し、このクロック発生回路3のクロック信号４ｃｋを１／４分周器4を介して、光電変換素子1にクロック信号ｃｋとして供給する如くする。

【００１１】また、この１／４分周器4の出力側に得られるクロック信号ｃｋをサンプリング信号として相関二重サンプリング回路2に供給する。この相関二重サンプリング回路2においては、フィールドスルー期間１ｂのレベルを基準レベルとし、信号期間１ｃのレベルをサンプリングホールドし図２Ｂに示す如く逆位相の周波数ｃｋでサンプリングされた離散的信号２ａを得る如くする。この相関二重サンプリング回路2の出力側に得られる離散的信号２ａを加算回路5に供給する如くする。

【００１２】また、6はディザ信号発生回路を示し、本

例においてはこのディザ信号として、図２Ｃに示す如く、図２Ｂに示す離散的信号２ａと同じ周期の鋸歯状波信号６ａとする。この鋸歯状波信号６ａのピークツウピークのレベルは後述するアナログ－デジタル変換回路８の１量子化レベル（ＬＳＢ）の３／４のレベルとする如くする。

【００１３】このディザ信号発生回路６の出力側に得られる離散的信号２ａと同じ周期の鋸歯状波信号６ａを加算回路５に供給する如くする。この加算回路５においては、この離散的信号２ａにディザ信号である鋸歯状波信号６ａが加算され、この加算回路５の出力側には図２Ｄに示す如く、この離散的信号２ａにディザ信号である鋸歯状波信号６ａが付加された信号が得られる。

【００１４】この加算回路５の出力側に得られる離散的信号２ａにディザ信号である鋸歯状波信号６ａが付加された信号をサンプリングホールド回路７に供給する。このサンプリングホールド回路７においては、クロック発生回路３に得られるクロック信号ｃｋの４倍の周波数のクロック信号４ｃｋをサンプリング信号として、サンプリングホールドし、このサンプリングホールド回路７の出力側に図２Ｅに示す如き１クロック信号ｃｋ期間に４回サンプリングホールドしたサンプリングホールド信号を得る如くする。

【００１５】このサンプリングホールド回路７の出力側に得られるサンプリングホールド信号をアナログ－デジタル変換回路８に供給する。このアナログ－デジタル変換回路８として、本例においては１０ビットの分解能のものを使用する。

【００１６】また本例においては、このアナログ－デジタル変換回路８は、クロック発生回路３に得られるクロック信号ｃｋの４倍の周波数のクロック信号４ｃｋでアナログ信号をデジタル信号に変換する如くする。

【００１７】従って、このアナログ－デジタル変換回路８の出力側には１クロック信号ｃｋ期間に４個の分解能が１０ビットのデジタル信号が得られる。このアナログ－デジタル変換回路８の出力側に得られる分解能が１０ビットのデジタル信号をデジタル積分回路９を構成する１２ビット構成のデジタル加算器９ａに供給する。

【００１８】このデジタル加算器９ａの出力信号をこのデジタル積分回路９を構成する１２ビット構成のデジタルのラッチ回路９ｂに供給し、このラッチ回路９ｂの出力信号をデジタル加算器９ａに供給する。このラッチ回路９ｂのクロック信号としてはクロック発生回路３に得られるクロック信号ｃｋの４倍の周波数のクロック信号４ｃｋにより動作させると共にクロック信号ｃｋをクリア端子ｃｌに供給し、これによりこのラッチ回路９ｂをクリアする如くする。

【００１９】即ちこのデジタル積分回路９は１クロック信号ｃｋ期間の４個のデジタル信号をデジタル積分する如くなしたものである。このデジタル加算器９ａの出力

信号を１２ビット構成のデジタル－アナログ変換回路を介して信号波形を観察したときは例えば図２Ｆに示す如き積分波形となる。

【００２０】このデジタル加算器９ａの出力信号を１２ビット構成のデジタルのラッチ回路１０に供給する。このラッチ回路１０にクロック信号として周波数ｃｋのクロック信号を供給する。即ちこのラッチ回路１０にはアナログ－デジタル変換回路８のデジタルの出力信号が４回積分された信号が順次供給されるものである。

【００２１】このラッチ回路１０の出力信号を１２ビット構成のデジタル映像信号出力端子１１に供給する如くする。このラッチ回路１０の出力信号を１２ビット構成のデジタル－アナログ変換回路を介して信号波形を観察したときには、図２Ｇに示す如く、図２Ｂに示す離散的信号２ａが１クロック信号ｃｋ期間遅れた信号に対応する信号が得られた。

【００２２】更に、図３及び図４を参照して、本例のこのアナログ－デジタル変換回路８、デジタル積分回路９及びラッチ回路１０の動作につき、模擬的に詳細に説明する。

【００２３】一般にアナログ－デジタル変換回路においては、図３に示す如く１サンプリング期間（１クロック信号ｃｋ期間）において、入力されるアナログ信号のレベルが１量子化レベル（ＬＳＢ）を越える毎にデジタル値が「１」ステップ上昇する。この分解能１０ビットのアナログ－デジタル変換回路８は１０２４ステップの分解能である。

【００２４】ところで本例においては、このアナログ－デジタル変換回路８の入力側に供給されるアナログ信号は相関二重サンプリング回路２の出力側に得られる離散的信号２ａにピークツウピークレベルが１量子化レベル（ＬＳＢ）の３／４のレベルのディザ信号としての鋸歯状波信号６ａが加算された信号であり、この１０２４ステップの夫々のステップ毎に図４Ａに示す如き４つの場合a_1～a_4が考えられる。

【００２５】即ち、場合a_1の如く、離散的信号２ａがあるステップの１量子化レベル（ＬＳＢ）の０～１／４のレベルのときはクロック信号ｃｋの４倍のクロック信号４ｃｋで順次４回C_1，C_2，C_3及びC_4、サンプリングホールド回路７でサンプリングホールドしても１回も１量子化レベルを越えない場合、場合a_2の如く、離散的信号が、あるステップの１量子化レベル（ＬＳＢ）の１／４～２／４のレベルのときで、１回越える場合、場合a_3の如く離散的信号が、あるステップの１量子化レベル（ＬＳＢ）の２／４～３／４のレベルのときで、２回越える場合及び場合a_4の如く、離散的信号が、あるステップの１量子化レベル（ＬＳＢ）の３／４～１未満のレベルのときで、３回越える場合である（図４Ｂ参照）。

【００２６】このアナログ－デジタル変換回路８の出力

をデジタル積分回路9で4回積分したときは、その成分値はアナログ的に見て、図4Cに如くなり、このラッチ回路10に得られるデジタル信号は、1024ステップの夫々のステップで4つの場合a_1～a_4の分解能を有する4096ステップのデジタル信号が得られ、分解能が12ビットのアナログ－デジタル変換回路と等価となる。

【0027】本例によれば、撮像信号を周波数ckでサンプリングした離散的信号2aに鋸歯状波信号6aのディザ信号を付加した後に、この離散的信号2aの周波数の4倍の周波数4ckのクロック信号を使用してアナログ－デジタル変換回路8でデジタル信号に変換しているので、この離散的信号2aの1周期で4個の10ビットのデジタル信号が得られ、この4個のデジタル信号をデジタル積分回路9で4回積分した後に出力するようにしているので、このアナログ－デジタル変換回路8の4倍の分解能即ち12ビットの分解能のデジタル信号が得られる。

【0028】本例によれば回路規模としては従来のアナログ－デジタル変換回路に比較し、デジタル積分回路9及びラッチ回路10が増加するだけなので、この回路規模の増加は比較的少なく、従って消費電力の増加も比較的少ない利益がある。この為本例によれば高分解能のアナログ－デジタル変換手段を比較的安価に実現できる。

【0029】また、本例によればアナログ－デジタル変換時にディザ信号を付加しているが、デジタル積分回路9で積分しているので、出力信号のゆらぎが生じない利益がある。

【0030】尚、図1においては、ピークツウピークが3／4LSBの鋸歯波信号6aを発生するディザ信号発生回路6を設ける如く述べたが、図5に示す如く、相関二重サンプリング回路2のホールド用コンデンサC_3に並列に抵抗器R_1を設け、このコンデンサC_3と抵抗器R_1とによる時定数をリップルが約3／4LSBとなる如くしても良い。

【0031】この図5につき更に述べるに、この図5において、20は相関二重サンプリングホールド回路2の入力端子を示し、この入力端子20に、図2Aに示す如き撮像信号を供給する。この入力端子20をこの撮像信号の基準信号であるフィールドスルー期間1bにのみオンする接続スイッチ21を介して撮像信号の信号期間1cにサンプリングパルスckによりオンするサンプリングスイッチ22aの一側に接続する。

【0032】この接続スイッチ21及びサンプリングスイッチ22aの接続点を基準電圧ホールド用のコンデンサC_1を介して接地する。このサンプリングスイッチ22aの他側を比較回路を構成する演算増幅回路23の非反転入力端子＋に接続すると共にこの非反転入力端子＋を基準電圧ホールド用のコンデンサC_3を介して接地すると共にこのコンデンサC_3に並列に時定数によるリップルが約3／4LSBとなる抵抗器R_1を接続する如くする。

【0033】また、この入力端子20を撮像信号の信号期間1cにサンプリングパルスckによりオンするサンプリングスイッチ22bを介して演算増幅回路23の反転入力端子－に接続すると共にこの反転入力端子－をサンプリングホールド用のコンデンサC_2を介して接続する。この演算増幅回路23より出力端子24を導出する。

【0034】この図5においては、入力端子20に図2Aに示す如き撮像信号を供給したときには、出力端子24には図2Dに示す如き、撮像信号の信号期間1cがサンプリングホールドされた離散的信号に鋸歯状波信号のディザ信号が付加された信号が得られる。

【0035】また、図1例ではサンプリングホールド回路7を設けたが、アナログ－デジタル変換回路8がフラッシュ型であったり、このアナログ－デジタル変換回路8内にサンプリングホールド回路を内蔵しているものでは、このサンプリングホールド回路7を省略できる。

【0036】また、上述実施例においては離散的信号の周波数ckの4倍の周波数のクロック信号でアナログ－デジタル変換する如く述べたが、このクロック信号の周波数はn倍（nは2以上の整数）のものが使用でき、このときはn倍の分解能とすることができる。

【0037】また、本発明は上述実施例に限ることなく本発明の要旨を逸脱することなくその他種々の構成が採り得ることは勿論である。

【0038】

【発明の効果】本発明によれば回路規模として、従来のアナログ－デジタル変換回路に比較し、デジタル積分回路9及びラッチ回路10を増加するだけの比較的少ない回路規模の増加で高分解能のアナログ－デジタル変換装置を得ることができる利益がある。

【0039】また本発明によれば回路規模の増加が少ないので消費電力の増加が少なく且つ安価に高分解能のアナログ－デジタル変換装置を得ることができる利益がある。また、本発明によればアナログ－デジタル変換時にディザ信号を付加しているが、デジタル積分器で積分しているので出力信号のゆらぎが生じない利益がある。

【図面の簡単な説明】

【図1】本発明デジタル信号処理装置の一実施例を示す構成図である。

【図2】本発明の説明に供する線図である。

【図3】説明に供する線図である

【図4】本発明の説明に供する線図である。

【図5】本発明の要部の他の例を示す構成図である。

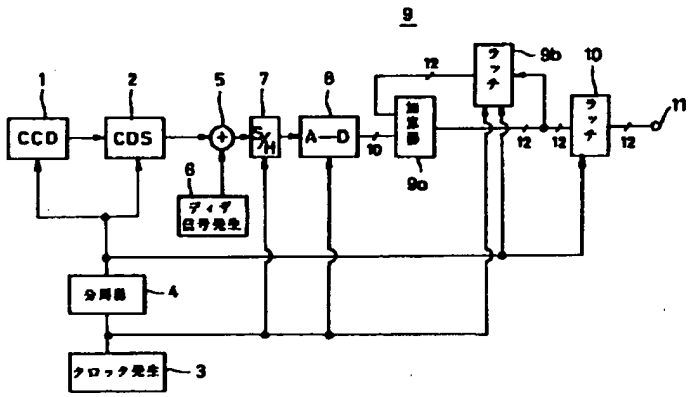
【符号の説明】

1　光電変換素子、2　相関二重サンプリング回路、3　クロック発生回路、4　1／4分周器、5　加算回路、6　ディザ信号発生回路、8　アナログ－デジタル

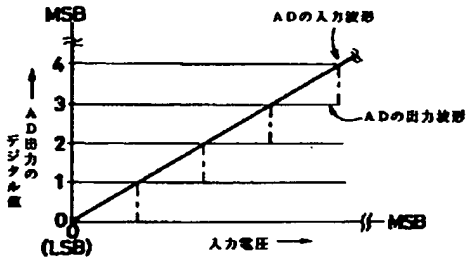
7　　8

変換回路、9　デジタル積分回路、10　ラッチ回路、　　11　出力端子

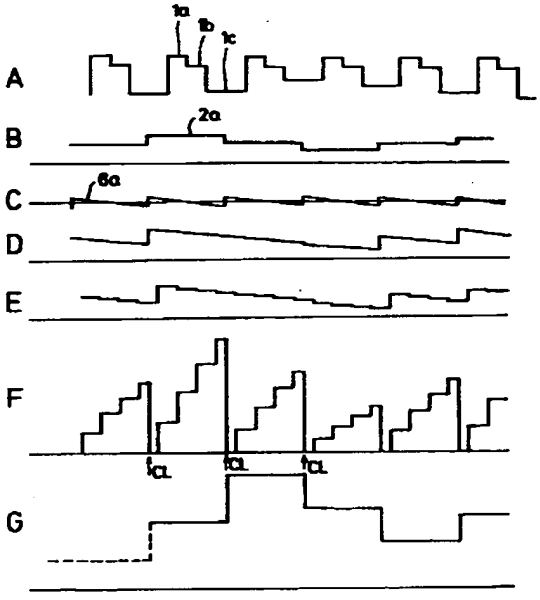
【図1】



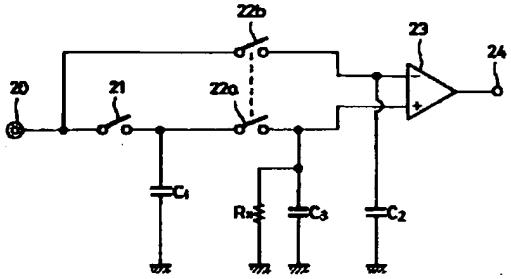
【図3】



【図2】



【図5】



【図4】